Low-Power STDR CMOS Sensor for Locating Faults in Aging Aircraft Wiring

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***Abstract*—A CMOS sensor used to locate intermittent faults on live aircraft wires is presented. A novel architecture was developed to implement the Sequence Time Domain Reflectometry method on a 0.5-μm integrated circuit. The sensor locates short or open circuits on active wires with an accuracy of +/-1 ft when running at a clock speed of 100 MHz. A novel algorithm is proposed that utilizes the shape of the correlation peak to account for sub-bit delay, thus increasing the accuracy of fault location. The power consumed by the microchip is 39.9 mW.**

***Index Terms*—CMOS sensor, pseudo-random noise, reflectometry methods, spread spectrum, wire fault location.**

I. Introduction

AGING electrical wiring systems have been identified as an area of critical national concern [1], [2]. For aircraft, where both preventative and responsive maintenance are taken very seriously, aging wiring is a very expensive problem. Electrical wiring problems in the U.S. Navy cause an average of two in-flight fires every month, more than 1,077 mission aborts, and over 100 000 lost mission hours each year [3]. Each year the Navy spends from one- to two-million man hours finding and fixing wiring problems [4]. A majority of the man hours spent locating faults are on intermittent faults that occur in flight but are not easily replicated on the ground. New "arc fault circuit breakers" (AFCI) have been developed that are capable of detecting the fault and tripping the circuit before severe damage is done. Although AFCIs will improve the safety of the aircraft, they promise to be a maintenance nightmare, as the faults left behind are too small to detect with typical fault location methods.

Reflectometry methods have been used to locate faults on wires for decades. These methods send a high frequency signal down the line, which reflects back at impedance discontinuities such as open or short circuits. The difference (time delay or phase shift) between the incident and reflected signal is used to locate the fault on the wire. The nature of the input signal is used to classify each type of reflectometry. Time Domain Reflectometry (TDR) uses a fast rise time pulse [5]. Frequency Domain Reflectometry (FDR)—including Phase Detection Reflectometry (PD-FDR) [6], [7], Mixed Signal Reflectometry (MSR) [8], and Standing Wave Reflectometry (SWR) [8]—uses sine wave signals to locate the fault on the wire. Multicarrier Reflectometry (MCR) uses a combination of sine waves with random phases [9]. Spectral Time Domain Reflectometry (STDR) uses a pseudo-noise (PN) code, and Spread Spectrum Time Domain Reflectometry (SSTDR) uses a sine-wave-modulated PN code [12]. It has been shown that reflectometry methods are not effective for location of small faults on aircraft wires, because the tiny reflections they return are smaller than the tiny reflections that are returned from other normal variations in the wire [10], [11]. The only way to locate these "small" faults, therefore, is to locate them when they are (intermittently) nearly open or short circuits. This requires a system that can continuously test the wires while they are live (and potentially in flight). STDR and SSTDR have been shown to be effective for location of intermittent faults on both analog (400 Hz) and digital (MilStd 1553) systems [12].

In this paper, we present the design and implementation of a stand-alone sensor system that can sense the nature of a fault in aircraft wiring both on the ground and in flight. The desired sensor system should not rely on the aircraft's power supply but should instead have its own power supply, preferably a small battery. This puts a severe power constraint on this sensor system, pressing the need for low power operation for longer battery life. Size and weight constraints, as well as the need for low-power operation, require an integrated circuit implementation of such a system.

The two reflectometry methods that show the promise of fault location on live aircraft wires, namely STDR and SSTDR, have not been implemented in silicon prior to this work. Out of these two methods, STDR is more suitable for low-power implementation, because it needs fewer power-hungry circuits (i.e., modulators and demodulators) than SSTDR for its realization. Hence, we chose STDR for integrated circuit implementation to locate faults on live wires, using a novel architecture called the Time Domain Vernier (TDV) method.

This paper describes the design of a CMOS integrated circuit for intermittent fault location on electrical wires using the TDV Method. Section II presents the TDV method. Section III describes the integrated circuit implementation, and Section IV describes the experimental results. Section V presents an algorithm to achieve higher accuracy of fault location, and Section VI concludes with an evaluation of next-generation design considerations.

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II. Time Domain Vernier (TDV) Method

A. Analytical Description

In the TDV method, a deterministic binary PN sequence is transmitted onto a wire on top of (and within the noise margin of) the existing aircraft signal. This PN code is a recursive linear sequence. ML codes are chosen for this application, since they have very strong autocorrelation and poor cross correlation, and can be generated with relatively simple digital hardware [13].

The PN sequence can be described as follows. Let b_n be a recursive linear sequence of period K consisting of 1s and 0s. Let a_n be a recursive linear sequence consisting of 1s and -1s such that

$$a_n = 2 \cdot b_n - 1. \tag{1}$$

Then let

$$s(t) = \sum_{n=-\infty}^{n=\infty} a_n \cdot p(t - nT_c) \tag{2}$$

where

$$p(t) = \begin{cases} 1, & 0 \le t \le T_c \\ 0, & \text{otherwise} \end{cases} \tag{3}$$

so that $s(t)$ is a Recursive Linear Signal (RLS) of period $T = KT_c$ consisting of 1s and -1s. Here, T_c is the minimum time step of 1 or -1, otherwise known as a "chip." Note that

$$s(t) = s(t + T) \tag{4}$$

for any RLS of period T.

The TDV test system transmits the signal $s(t)$ onto the cable, where it is reflected by the impedance discontinuity (open or short) in the cable. Let $s'(t)$ be the reflected signal, which is a scaled and time delayed copy of the transmitted signal $s(t)$. The reflected signal $s'(t)$ will return to the test system after some transmission delay. The cross correlation of the transmitted sequence $s(t)$ and the reflected sequence $s'(t)$ is a function of the delay of the reflected sequence and can be written as

$$R_{ss'}(\tau) = \frac{1}{T} \int_0^T s'(t) s(t + \tau). \tag{5}$$

As seen in (5), the value of cross correlation $(R_{ss'}(\tau))$ is maximum at the instant when both $s'(t)$ and the time shifted copy of $s(t)$ are perfectly aligned with each other (i.e.,τ is equal to the delay of the reflected signal $s'(t)$). This delay (τ) of the reflected signal can be translated into the distance to the fault (d) by the following relationship:

$$2d = \text{VOP}\tau \tag{6}$$

where "τ" is the delay of the reflected PN sequence, VOP is the velocity of propagation on the cable, and d is the distance to the fault.

The cross-correlation function in (5) is essentially a delay-multiply-integrate operation. A copy of the transmitted sequence is delayed, multiplied to the reflected signal, and the product of these signals is integrated over one signal period T. In the TDV algorithm, we generate a copy of the transmitted PN signal called the Vernier signal, or reference signal, and use this signal for computing the cross-correlation function $R_{ss'}(\tau)$. Every time the Vernier PN sequence repeats (T), a 1-bit time delay is added, so that the Vernier sequence lags the transmitted PN sequence. This "lagging" PN sequence is multiplied by the reflected signal, and the resultant product is integrated over the signal period T. As the Vernier sequence repeats itself, the delay between the Vernier PN sequence and the transmitted PN sequence increases. The next section on the architecture of the TDV method details how the cross-correlation function $R_{ss'}(\tau)$ is computed in the TDV system.

Like all reflectometry methods, the Vernier sequence method measures time delay between the incident and reflected signals. This is converted to a measurement of distance to the fault by multiplying it by the velocity of propagation (VOP). The VOP depends on the type of wire (which may or may not be known) and its orientation relative to other metallic structures (which is typically nonuniform and unknown). VOP is typically near 2/3 the speed of light for aircraft wiring, and may vary by about +/-10%. Any error in VOP translates directly to error in distance measurement, regardless of the type of reflectometry used.

Another issue that impacts the resolution of reflectometry approaches is the occurrence of multiple reflections. In addition to the first reflection from the mismatch between the tester and wire and the second reflection from the end of the wire, reflections occur at branches and junctions in wires and any other impedance discontinuity on the wire. This creates a set of reflections, some of which may be overlapped. This is confusing at best and difficult or impossible to fully resolve from a single test point. Measurement errors are almost always worse with multiple reflections than without, and the precise degradation depends on the configuration of the system. Methods to identify the source of multiple reflections have been developed and significantly improve this situation [17].

B. Architecture

Fig. 1(a) shows a block diagram of a TDV method. Point A shows the output of the PN sequence generator, which is a K-bit long maximum length PN signal given by (2). Fig. 1(b) shows the relevant waveforms in this system for a simple illustrative case using a PN sequence of length $K = 3$ (In our actual implementation, we use a much longer PN sequence with $K = 1023$). In the simplified example of Fig. 1(b), the PN signal consists of three bits: $\{1, -1, 1\}$. The PN sequence generator is capacitively coupled to the cable as shown in Fig. 1(a). The capacitor serves two purposes. First, it protects the TDV test system from the low-frequency, high-voltage aircraft power signal by filtering it out. It also provides a high impedance coupling to the cable to minimize coupling-induced reflections in real wiring situations.

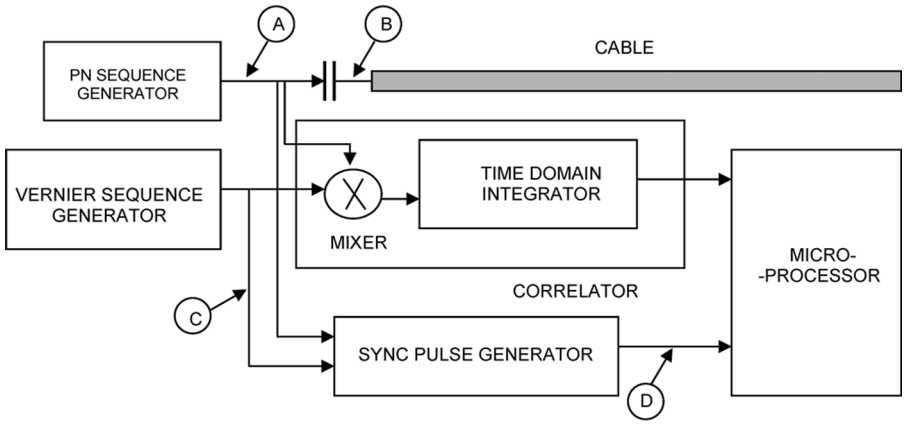

Fig. 1. (a) Block diagram of TDV method.

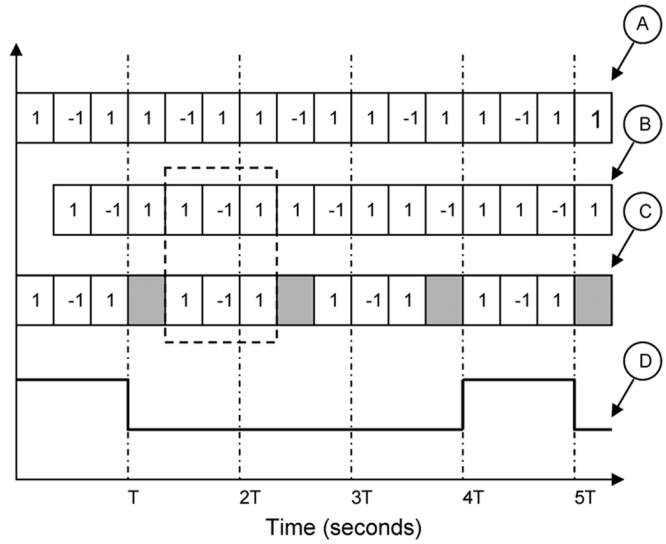

Fig. 1. (b) Waveforms in the proposed TDV system for a simple case where $K = 3$.

Point C in Fig. 1 is the output of the Vernier signal generator (i.e., reference signal) which is the same as the PN sequence, except that the last bit is repeated once at the end of the sequence. This additional bit is shown in gray in Fig. 1(b). Thus, the Vernier signal is delayed by one bit each time the sequence is completed (For example, the Vernier signal is delayed by one bit after the first sequence period, two bits after the second sequence period, and three bits after the third sequence period is completed). It is aligned with the PN signal after the $K + 1$ sequence repetitions, and the cycle begins again. Thus, the Vernier signal acts as the delayed version of the transmitted signal (delayed in steps of one bit) needed to compute the cross-correlation function $R_{ss'}(\tau)$. The Vernier sequence is always delayed in discrete, 1-bit steps so that this delay can be well controlled by the on-chip clock. Had the delay of the Vernier sequence been an arbitrary continuous-time delay, its value would be subject to temperature and process variations.

The Vernier sequence provides delays in increments of one bit of the PN signal. The accuracy of fault location is directly proportional to the width of the single bit of the PN sequence. To illustrate this, let us assume that the reflected PN sequence has a delay of one bit where the width of each bit is 10 ns. Using (6) with $\tau = 10$ ns and VOP $= 2 \times 10^8$ m/s, one bit of delay corresponds to $d = 3$ ft of cable length. Now if the width of one bit of the PN sequence is reduced to 5 ns, then using (6) with $\tau = 5$ ns and VOP $= 2 \times 10^8$ m/s, one bit of delay corresponds to $d = 1.5$ ft of cable. Thus, the smaller the width of one bit of PN sequence (i.e., the higher the frequency of the input clock for the PN sequence generator), the better the resolution of the fault detection system. For an accuracy of 1 ft, by (6), we need the bit width to be 3.33 ns (i.e., an input clock of 300 MHz). Power consumed by digital circuitry is directly proportional to the clock frequency (i.e., the chip rate of the PN sequence). In this paper, we propose a method whereby accuracy of fault location down to 1 ft can be achieved using a chip rate of only 100 MHz.

Point D in Fig. 1(a) represents the output of a Synchronous Pulse Generator block. As shown in Fig. 1(b), the output of this circuit remains high for one sequence length when both the PN and Vernier sequences are aligned in time. This alignment occurs after every $K + 1$ sequences. The pulses generated by the Synchronous Pulse Generator provide the time reference for determining the delay between the initial (transmitted) signal and the reflected signal. The rising edge of the synchronization pulse denotes the beginning of the zero reference for the time axis of the correlator output. The delay between transmitted and reflected signal is proportional to the distance to the fault, and this distance can be determined using the known velocity of propagation on the line as shown in (6).

Point B in Fig. 1(a) shows the PN sequence reflected at the open-circuited end of the cable. In this example, we assume that the delay due to the attached cable is exactly one bit long, as shown in Fig. 1(b). The dashed box in Fig. 1(b) shows that the reflected sequence is perfectly aligned with the second Vernier sequence which has a delay of one bit compared to the transmitted PN sequence. The magnitude of the correlation of the reflected sequence and Vernier sequence is maximum at this point of perfect alignment.

The time difference between the location of the correlation peak and the falling edge of the Synchronization (Sync) Pulse when normalized by time T (the period of the PN sequence)

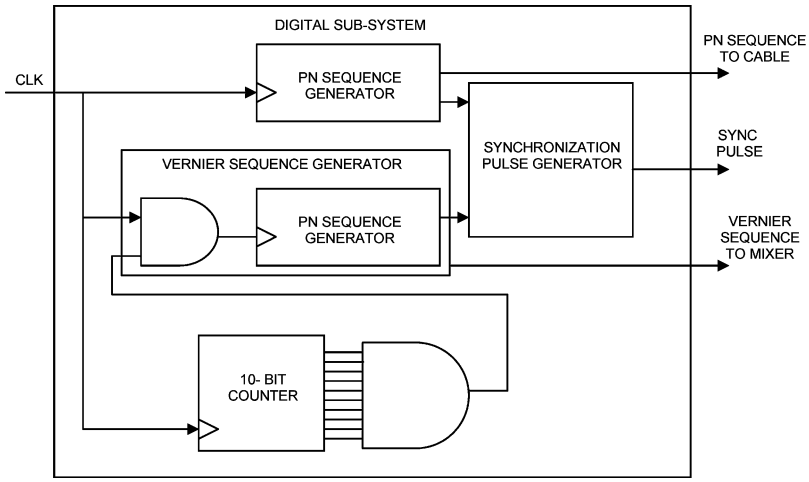

Fig. 2. Digital subsystem of TDV system.

gives us the delay of the reflected PN signal on the cable (τ). This delay (τ) can be translated into the distance to the fault by noting that the TDV method transforms a 1-bit delay in the reflected sequence into a K-bit delay between the Sync Pulse and the point of maximum correlation. Thus, the correlator signal can be sampled using a relatively slow (and, thus, low power) analog-to-digital converter.

Since the reflected signal will likely be attenuated and noisy, unlike the ideal reflection shown in Fig. 1(b), the proposed architecture uses analog correlation between the Vernier sequence and the reflected signal to measure the delay of the reflected sequence. One alternative to using analog correlation would be to use digital matched filters (DMFs) to detect the delay of the reflected sequence [14]. The DMF approach is not suitable for this application, as it would require high-speed sampling and, thus, a high performance analog-to-digital converter, which translates to larger power consumption. Additional on-chip memory would also be required to store sequences with many different delays to be used in the filter, and this would require fast, power-hungry static RAM cells.

III. Integrated Circuit Implementation

The TDV architecture described in the previous section was implemented in a mixed-signal integrated circuit using a commercially available three-metal, two-poly 0.5-μm CMOS process. The chip uses both digital and analog components in its operation. The digital subsystem is shown in Fig. 2, and consists of a PN sequence generator, a Vernier sequence generator, a 10-bit counter, and a SPG.

The PN sequence generator is implemented using a 10-bit Linear Feedback Shift Register (LFSR). The Vernier sequence generator is identical to the PN sequence generator except that the clock input to the flip flops of the LFSR is logically ANDed with a "stall" signal generated by the 10-bit counter. This signal stalls the Vernier sequence generator for one clock cycle at the end of a sequence (repeating the last bit), and introduces a 1-bit delay in the Vernier sequence each time the 1023-bit sequence is completed. Thus, the Vernier sequence is initially synchronized with the main PN sequence generator but lags by one bit after the sequence is repeated for the first time, then lags by two bits after the sequence is repeated the second time, and so on. Eventually, the Vernier sequence lags by 1023 bits and is once again synchronized with the PN sequence generator. In this way, the Vernier sequence generator repeatedly produces all possible delayed versions of the PN sequence (assuming only integer delays).

Although the present architecture of the TDV system repeats the Vernier sequence 1023 times, this is not actually needed for typical aircraft wires with a maximum length of 100 ft. For instance, if the input clock frequency of 100 MHz is used, then one bit of delay corresponds to $d = 3$ ft of cable length. A 100-ft cable can be scanned by repeating the Vernier sequence 34 times. Thus, future versions of the TDV integrated circuit implementation will reset the Vernier sequence after generating all possible integer delays (34 delays) adding up to 100 ft of cable length.

The Synchronization Pulse Generator (SPG) is implemented using an RS flip flop which generates a pulse that stays high for one complete PN sequence duration when both the PN sequence and the Vernier sequence are aligned (i.e., zero delay). Fig. 3 shows a block diagram of the analog subsystem of the chip that performs the correlation between the Vernier and reflected sequences. The correlator consists of a mixer (for multiplication) and two first-order low-pass $G_m - C$ filters (for integration).

Fig. 4 shows the schematic of the Gilbert-cell mixer from Fig. 3. The mixer takes two differential voltage inputs X and Y. The output current I_{out} is proportional to the product of the two differential input voltages. The sequence reflected from the end of the cable is applied to the X input, and the Vernier sequence is applied to the Y input. The $G_m - C$ filter uses a current-mirror operational transconductance amplifier (OTA) whose transconductance (G_m) is adjustable by changing its bias current. By varying the G_m of a filter, its cutoff frequency can be varied. The time constants of the integrator can be tuned by adjusting the amplifier bias current, which is controlled using off-chip resistors.

Fig. 5 shows a microphotograph of the integrated TDV chip after fabrication. The total die area is 1.5×1.5 mm^2, but the total active circuitry area is only 0.192 mm^2. The digital subsystem consumes 80% of the layout area. The power consumed by the

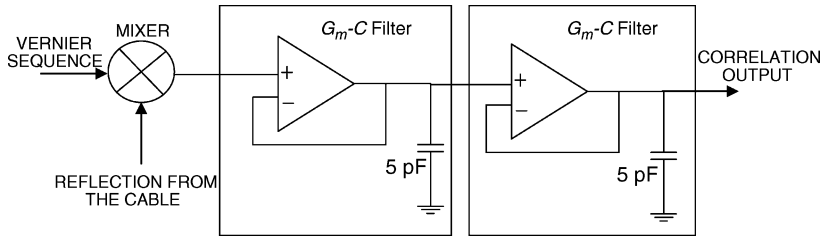

Fig. 3. Analog subsystem of TDV system.

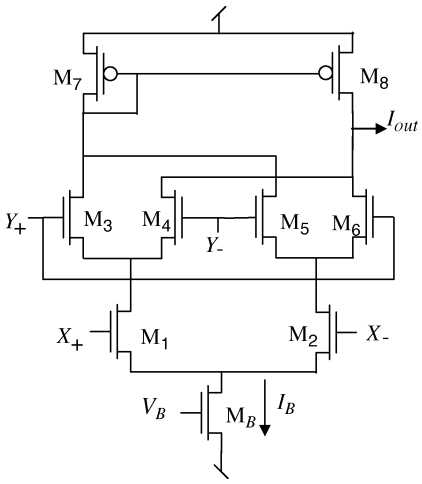

Fig. 4. Gilbert-cell mixer used in the correlator.

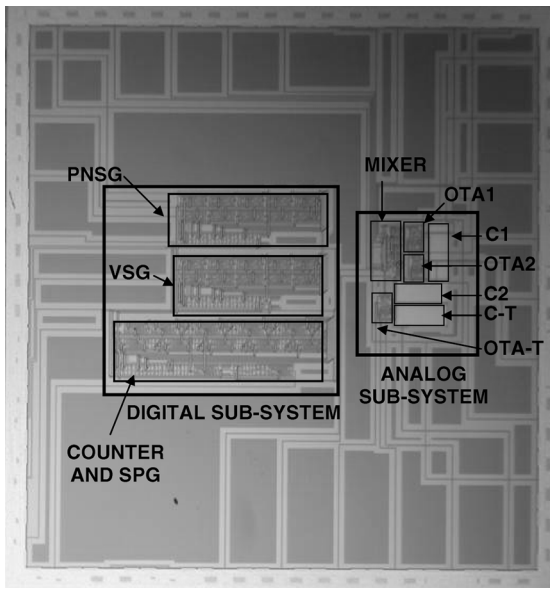

Fig. 5. Chip microphotograph of the TDV system. Total die area is 1.5×1.5 mm^2. PNSG: PN sequence generator. VSG: Vernier sequence generator. SPG: synchronization pulse generator. OTA: operational transconductance amplifier. (OTA1 + C1): first low-pass filter. (OTA2 + C2): second low-pass filter. (OTA-T + C-T): filter test structure.

CMOS integrated circuit is 52.8 mW at 100-MHz clock speed. Out of this power, 12.9 mW was consumed in driving internal diagnostic signals off chip for testing. These signals would not be needed in the final version of the microchip, so the power needed for the sensor is only 39.9 mW. Of this power consumed by the chip core, 35.7 mW is consumed by digital circuitry and 4.2 mW is consumed by analog circuitry.

IV. Measured Results

THE chip was tested on a custom-made printed circuit board using a clock frequency of 100 MHz. Thus, the width of one bit of the PN sequence is 10 ns, and the total 1023-bit PN sequence has a period of 10.23 μs. Using (6) with $\tau = 10$ ns and VOP $= 2 \times 10^8$ m/s, one bit of delay corresponds to $d = 3$ ft of cable length.

When there is an open circuit, the output of correlation is a positive peak. For a short circuit, the output of correlation is a negative peak. As the correlation peak is sampled, the value of maximum valued sampled is stored and the value of the minimum valued sample is stored. If the ratio of the maximum valued sample to the minimum valued sample is less than one, then the fault is short circuit otherwise it is an open circuit.

In order to distinguish the peak in the correlation waveform due to an open or a short from the noise present in the correlation waveform, a threshold value is chosen to determine the existence of a peak due to a fault on the cable. The value of this threshold for detecting a peak due to open or short circuit is decided by the noise floor. In this case, it was chosen as +/-25 mV, which is fairly conservative as the noise present on the measured correlation waveform is not more than +/-10 mV.

The exact shape of the correlation signal depends on the time delay between the transmitted and reflected signals, as the following examples illustrate. Fig. 6(a) shows the simulated (dashed line) and measured results for the case when the length of the open-circuited wire produces a delay of 29 bits ($\sim$87.75 ft) between the transmitted code and reflected code (Note that it was not practical to fully simulate the TDV circuit in SPICE due to the long simulation time required for the 1023-bit sequences. Hence, a higher-level model in MATLAB was created to produce the simulation results shown here).

For ML sequences, the shape of the correlation peak is triangular if an ideal integrator is used for correlation [13]. The shape of correlation peak in Fig. 6(a) is rectangular, because a first-order IIR filter was used to realize a first-order RC low-pass filter (leaky integrator similar to one used on the integrated circuit) with a cutoff frequency equal to $1/T$ (T is the period of the PN signal). Moreover, in simulation, it is assumed that there is no attenuation of the transmitted signal which is reflected back by the impedance discontinuity on the cable. Thus, the reflected signal is an unattenuated and time delayed copy of the transmitted signal. When the reflected and the Vernier

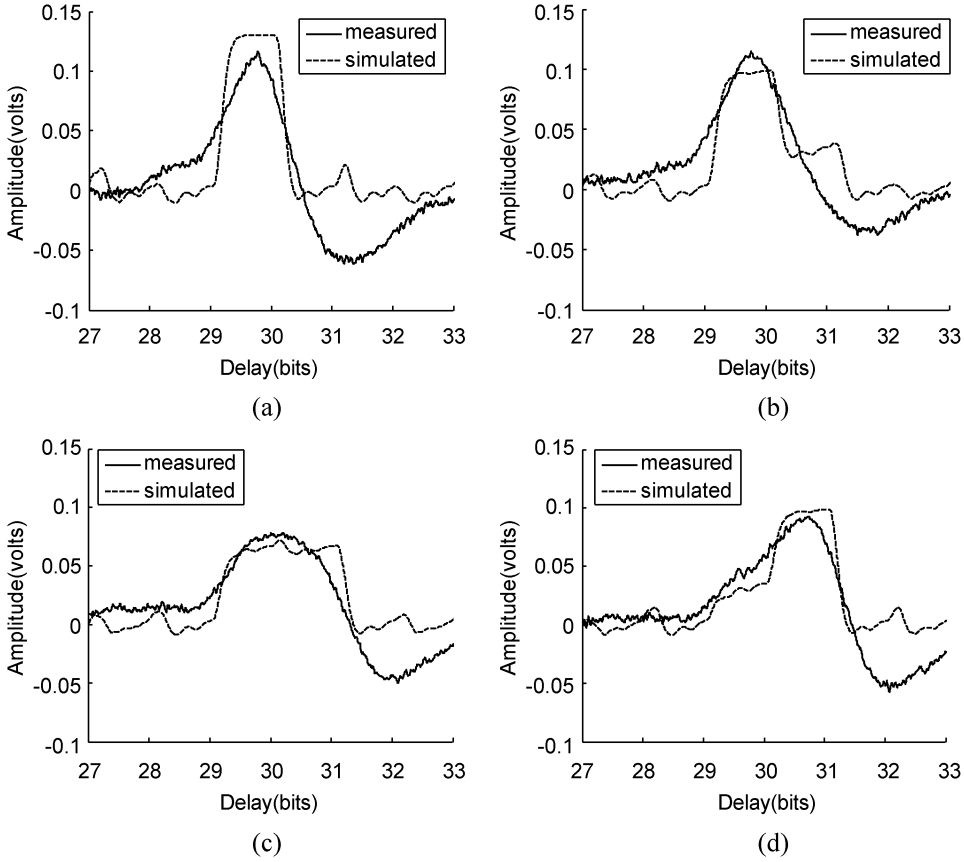

Fig. 6. Correlator outputs for (a) integer bit delay and (b)–(d) sub-bit delays. (a) Correlator output for 29-bit delay $(87.75')$. (b) Correlator output for 29.25-bit delay $(88.5')$. (c) Correlator output for 29.5-bit delay $(89.25')$. (d) Correlator output for 29.75-bit delay $(90')$.

signal start aligning, the RC low-pass filter used in simulation reaches its maximum value (saturates) very quickly, and, hence, the simulated shape of the correlation peak in Fig. 6(a) appears rectangular.

The measured correlation output of the TDV system in Fig. 6 exhibits undershoot, after the peak of correlation. This undershoot is observed in STDR systems due to capacitive coupling of the PN signal to the cable under test [15]. The capacitive coupling is needed to protect the circuit from the signals already on the wire under test.

Fig. 6(b)–(d) shows simulated (dashed line) and measured results for the cases where the open-circuit fault gives delays of (a) 29.25 bits (88.5 ft), (b) 29.5 bits (89.25 ft), and (c) 29.75 bits (90 ft), respectively. Similar results occur for short circuits, but the correlation peaks are inverted. It is clear that the shape of the correlation signal in each of Figs. 6(a)–(d) is different. The simplest method for calculating distance to wire fault is to simply measure the point where the correlation attains its highest value. Fig. 7(a) shows the fault location computed using simple peak detection in an experiment where an open-circuited cable was cut from a length of 99 ft to a length of 87 ft in steps of 1 in. The distance to the fault was estimated by measuring the time between the Sync Pulse and the correlation peak from the chip.

The two dashed lines in Fig. 7 enclose the deviation of data from its expected value, indicating the error in determining the location of fault on the cable. Since the 100-MHz clock limits our measurement precision, the error can be as large as 2.1 ft of

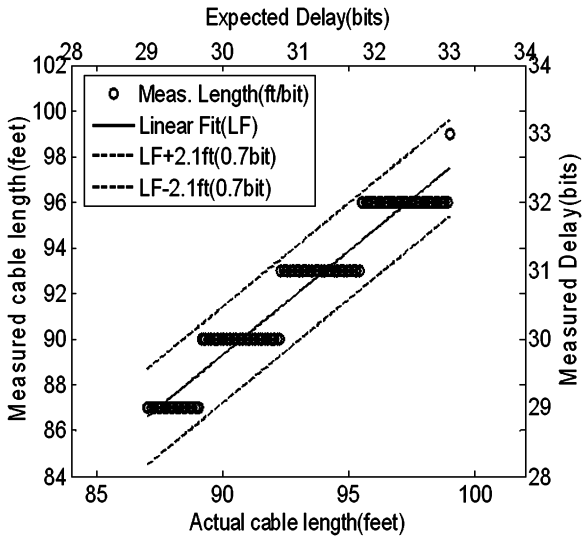

Fig. 7. Observed error in fault location using simple peak detection [dashed lines represent the maximum error +/-2.1 ft (+/-0.7 bit)].

the cable length from its expected value. The top and right axes in Fig. 7 show the delay in terms of the number of bits of the PN sequence. It assumes that one bit of delay equals 3-ft distance on the cable. As shown by the two dashed lines in Fig. 7, the error in determining the delay can be as large as 0.7 bit. Thus, determining the distance to a fault by measuring the position of

the highest value of the correlation output could result in error as large as 0.7 bit (or 2.1 ft at 100 MHz). The error in distance estimation could be reduced by using a faster clock, but this would result in greater power dissipation. Instead, an algorithm was developed to give "sub-bit" accuracy by utilizing the analog waveform information visible in the correlator signals of Fig. 6. The relationship between the shape of the correlation output peak and the accuracy of fault location is explored in detail in the next section.

V. Analyzing Results to Increase Accuracy of Fault Location

The delay of the reflected signal can be an integral or partial number of bits. Thus, the variable τ in (5) can assume any value. That is, τ is not constrained to be an integer multiple of T_c. The value of cross-correlation function $R_{ss'}(\tau)$when the delay is not an integer multiple of one bit $(T_c)$is provided by [16]. Substituting (2) into (5) yields

$$R_{ss'}(\tau) = \frac{1}{T}\sum_{m}\sum_{n} a_m a_n \int_0^T p(t-mT_c)p(t+\tau-nT_c)dt. \tag{7}$$

The integral in (7) is nonzero only when $p(t-mT_c)$ and $p(t+\tau-nT_c)$ overlap. The delay τ can be expressed as $\tau = kT_c+\tau_\phi$, where $0 \le \tau_\phi < T_c$. Using this substitution, the pulses overlap only for $n = k+m$ and $n = k+m+1$, so that (7) becomes

$$\begin{aligned} R_{ss'}(\tau) &= R_{ss'}(k,\tau_\phi) \\ &= \frac{1}{N}\sum_{m=0}^{N-1} a_m a_{k+m}\frac{1}{T_c}\int_0^{T_c-\tau_\phi} p(\lambda)p(\lambda+\tau_\phi)d\lambda \\ &\quad + \frac{1}{N}\sum_{m=0}^{N-1} a_m a_{k+m+1}\frac{1}{T_c}\int_{T_c-\tau_\phi}^{T_c} p(\lambda)p(\lambda-T_c+\tau_\phi)d\lambda \end{aligned} \tag{8}$$

where the substitution $\lambda = t - mT_c$ has also been employed. The discrete periodic cross-correlation function of two codes b_n and b'_n is defined by [16]

$$\theta_{bb'}(k) = \frac{1}{N}\sum_{n=0}^{N-1} a_n a'_{n+k} \tag{9}$$

where $a_n = 2\cdot b_n - 1$. Using this definition, the cross-correlation function $R_{ss'}(\tau)$ becomes

$$\begin{aligned} R_{ss'}(\tau) &= R_{ss'}(k,\tau_\phi) \\ &= \left(1-\frac{\tau_\phi}{T_c}\right)\theta_{bb'}(k) + \frac{\tau_\phi}{T_c}\theta_{bb'}(k+1) \end{aligned} \tag{10}$$

Equation (10) gives the relationship between the correlation output $R_{ss'}(\tau)$ in terms of the sub-bit (sub-chip) delay τ_ϕ and the integer delay k. The location of the fault on the cable is determined from the time delay observed when the correlation is maximum. Using simple peak detection limits the accuracy of the solution to at least 0.7 bit delay (or 2.1 ft at 100 MHz), as seen in Fig. 7. However, using the shape of the sub-bit delayed correlations, it is clear that additional accuracy can be obtained. This can be done efficiently with simple digital hardware, as follows.

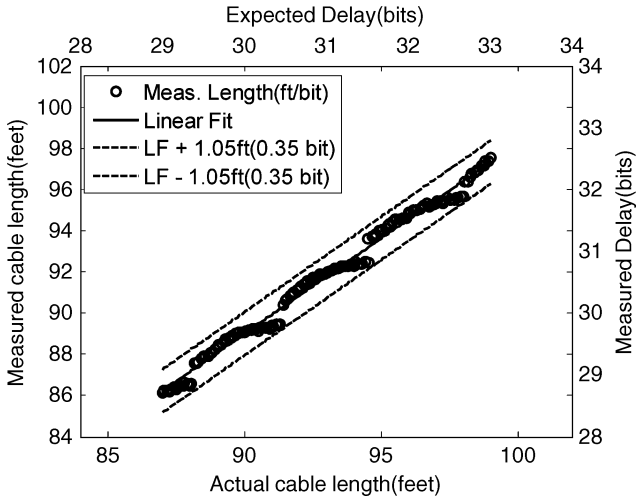

Fig. 8. Observed error in fault location taking shape of correlation peak into account [dashed lines represent the maximum error +/- 1.05 ft (+/- 0.35 bit)].

The correlation output is sampled with a frequency of $1/(T+(T/K))$, where T is the period of K bit long PN sequence. Three samples centered in time around the correlation peak are stored in the internal registers of a microprocessor that is digitizing the analog correlator output of the chip. The second sample is the highest valued (maximum) sample, the first sample is $T+(T/K)$ seconds before, and the third sample is $T+(T/K)$, seconds after.

Sub-bit fault location accuracy can be obtained using the following algorithm.

1) Normalize all three samples by the magnitude of the highest sample (i.e., the second sample).
2) Compare the normalized magnitudes of the first and third samples. Assign the greater magnitude to a variable h.
3) If the first sample is greater than the third sample, then subtract $(h/1+h)$ from the delay of the highest valued sample.
4) If third sample is greater than the first sample, then add $(h/1+h)$ to the delay of the highest valued sample.

For a short circuit condition, the algorithm is the same, except that the minimum value is used rather than the maximum, and values are compared to see which one is less than the other.

Whether the fault is an open or a short is determined by looking at the ratio of the maximum valued sample to the minimum valued sample. If this ratio is less than or equal to one, the fault is a short circuit; if it is greater than one, it is an open circuit. Fig. 8 shows the fault location estimated from the output of the TDV chip by taking the shape of correlation simple peak into account for an open-circuit cable cut from 99 to 87 ft in steps of 1 in. The two dashed lines in Fig. 8 enclose the deviation of data from its expected value, indicating the error in determining the location of fault on the cable. The maximum error observed was 1.05 ft. The top and right axes in Fig. 8 show the delay in terms of the number of bits of the PN sequence. It assumes that

one bit of delay equals 3-ft distance on the cable. As shown by the two dashed lines in Fig. 8, the error in determining the delay can be as large as 0.35 bit. Thus, there is an improvement by a factor of two over simple peak detection when the sub-bit delays are taken into account using this simple algorithm. Additional improvement is likely to be possible with better fit between the algorithm and sub-bit delay pulse shape.

VI. Conclusion

This paper describes the design and implementation of an integrated CMOS sensor to locate faults in live aircraft wiring. This was accomplished using the proposed novel architecture called the TDV method. This method is based on STDR with an additional bit delay at the end of each PN sequence. As a part of the system, the TDV method was implemented in a CMOS integrated circuit. The correlation output of this integrated circuit encodes the location of the fault on the line in time, and is slow enough to be sampled by an audio-frequency analog-to-digital converter despite the front-end system running at 100 MHz. A simple algorithm was proposed that utilizes the shape of the correlation peak to account for sub-bit delay, increasing the accuracy of fault location from 3 to 1.05 ft with no increase in clock speed. This algorithm is simple enough to be implemented on a small microcontroller. Thus, a small microcontroller with a slow analog-to-digital converter could be used to analyze the correlation output from the chip and determine location of the fault.

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